Signal and Power Integrity (SI/PI) Design for Advanced Packages

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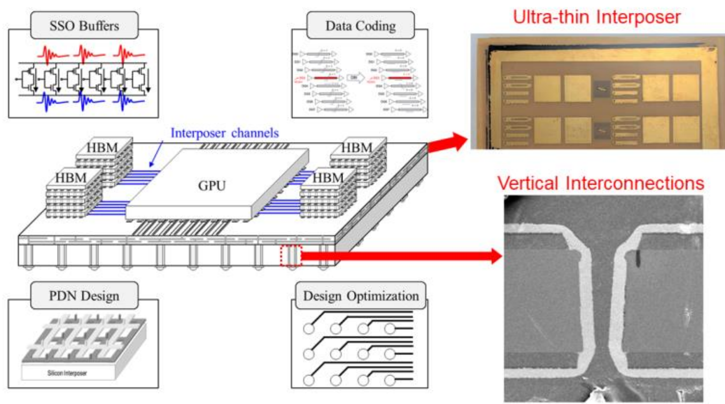
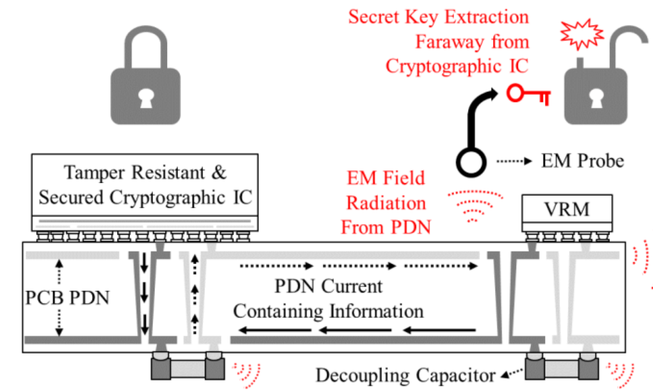
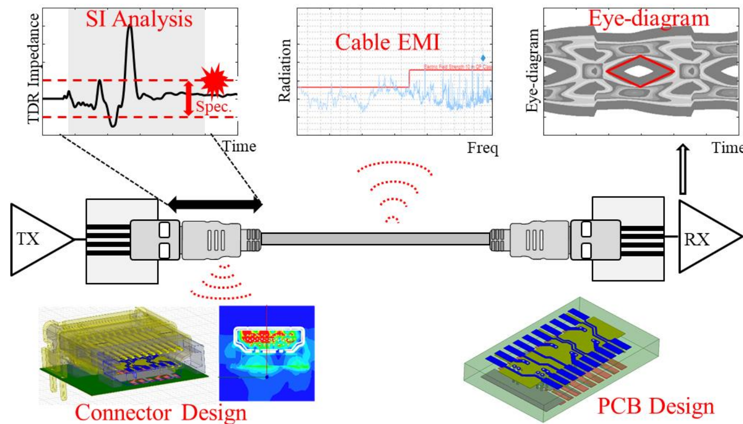
Packaging and Interconnection for “X” (PI4X)



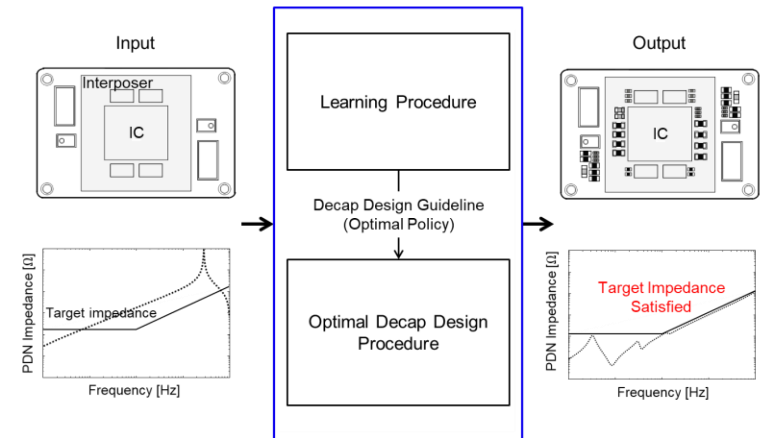
<Advanced Packaging for 2.5D/3D Integration>



<Hardware Security based on EMC/Packaging/Circuit Theory>



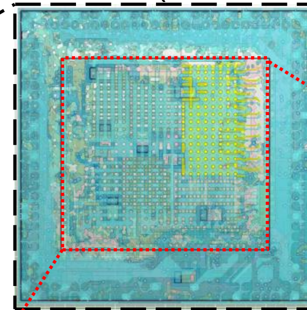
<Realization of low-noise interconnections and systems>



<Deep learning based Electrical Design Automation (EDA)>

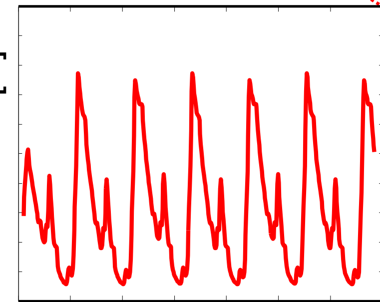
Chip-Package-PCB CoDesign for Mobile AP GPU (1)

< Package Model (+PKG EPS Cap) >



< System Board Model>

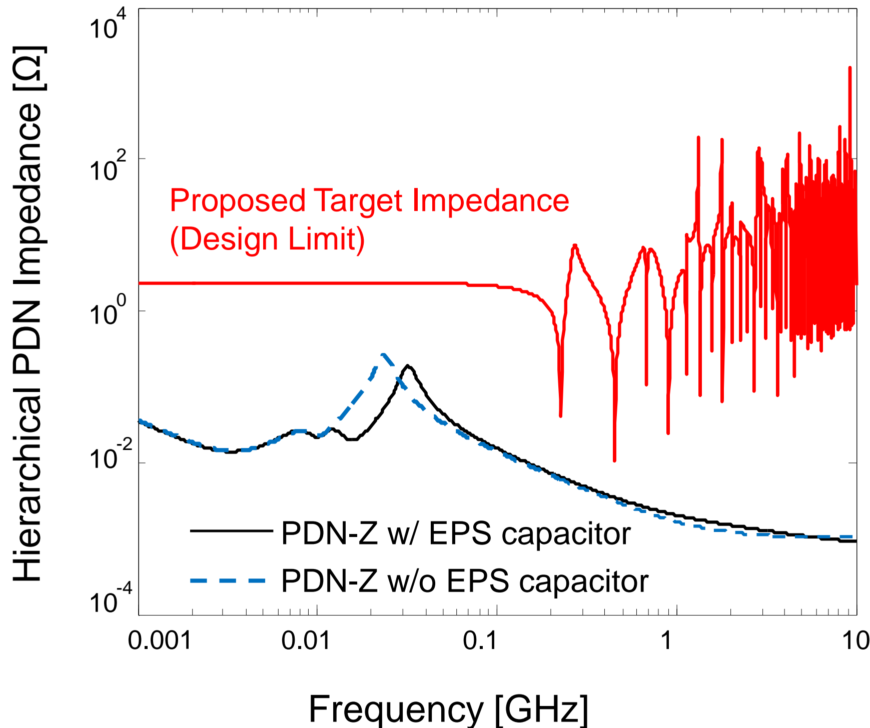
```
R_4_4 n960 VDD_1 33.6151765386
L_5_4 VDD_3 n961 5.0341904875e-09
R_5_4 n961 VDD_1 18.2853827768
R0_5 VDD_3 VDD_2 0.48905377884
L_1_5 VDD_3 n962 2.06078655324e-12
R_1_5 n962 VDD_2 0.301894905062
L_2_5 VDD_3 n963 3.5613154691e-10
R_2_5 n963 VDD_2 8.52692927719
L_3_5 VDD_3 n964 1.41063901928e-09
R_3_5 n964 VDD_2 12.2502842883
L_4_5 VDD_3 n965 2.53105281478e-09
R_4_5 n965 VDD_2 12.4514029115
L_5_5 VDD_3 n966 1.28595217346e-09
R_5_5 n966 VDD_2 4.73672850713
C0_6 VDD_3 0 4.05794323476e-11
```

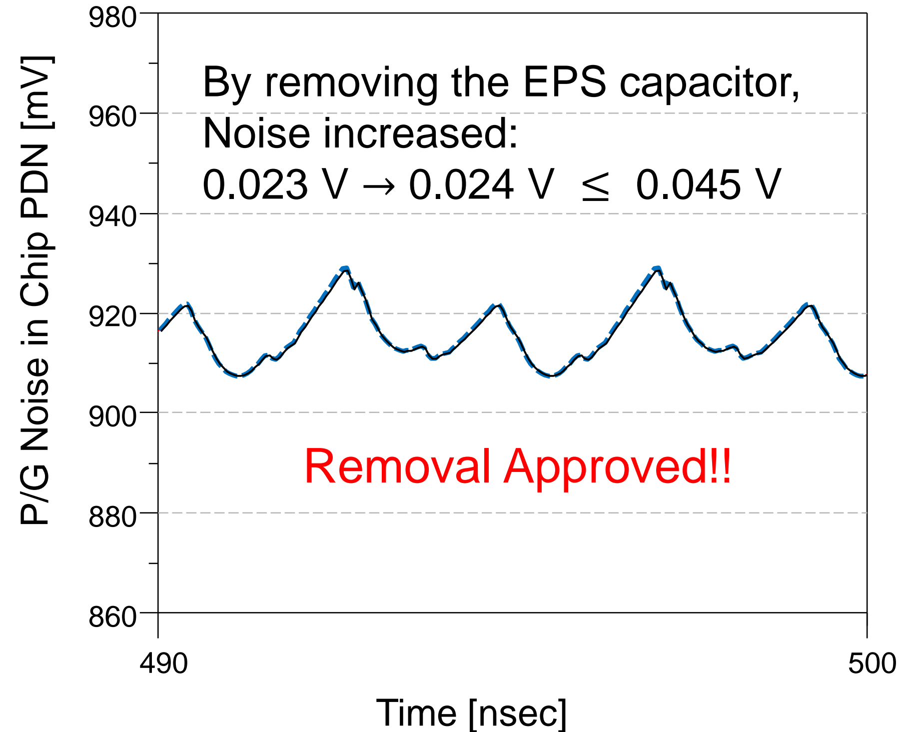


< On-chip Network + GPU Behavior Model>

- GPU PDN is constructed by system board, PKG, and chip PDN.
- In the SPICE, PWL current model is merged with the PDN Model (CPM + Network (PKG and Board)) for a system level simulation.

Chip-Package-PCB CoDesign for Mobile AP GPU (2)



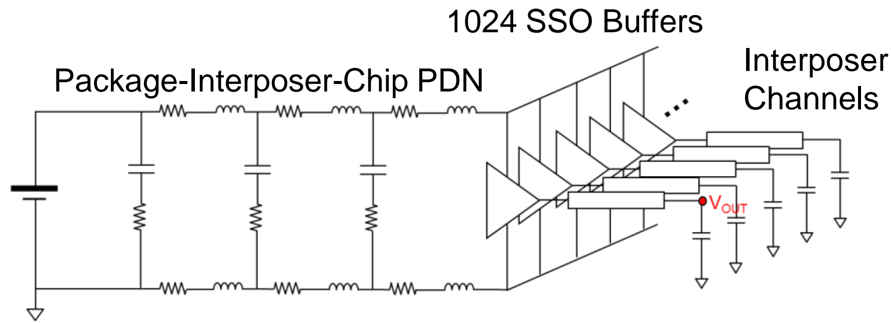


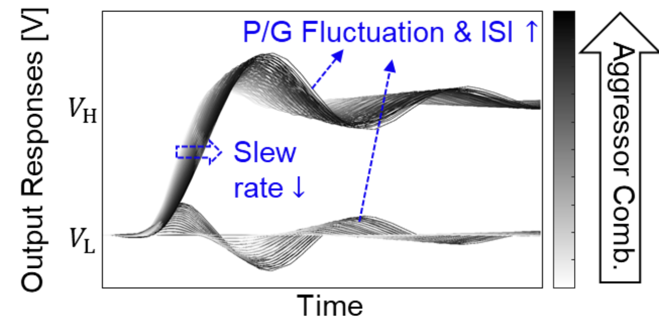
- There were three EPS capacitors in the package (CPU, GPU, LPDDR). Each increased the package cost 50 %.

- Proper SI/PI design has impacts on not only performance but also cost.

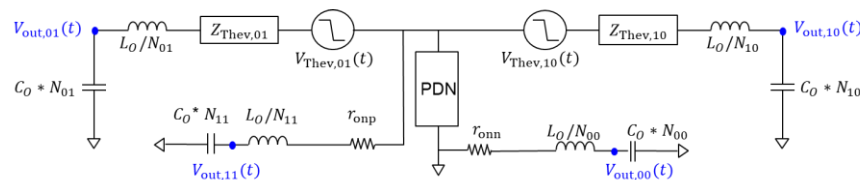
[Ref] Y. Kim et al., "Design of a Mobile AP GPU PDN based on Chip Power Model and Measurement", DesignCon 2016.

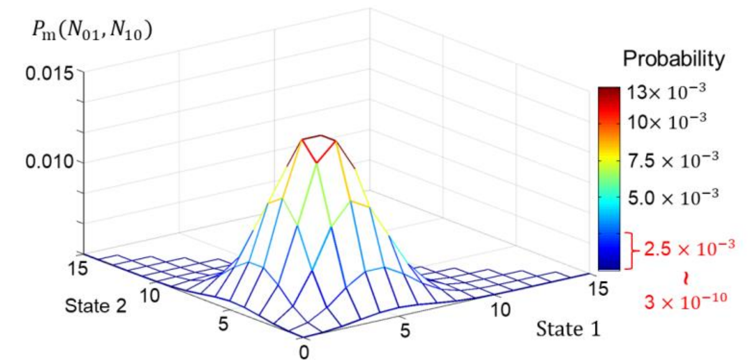
Statistical SI/PI Evaluator Development for HBM Interposer Channel (1)





Equivalent circuit & analytical formula



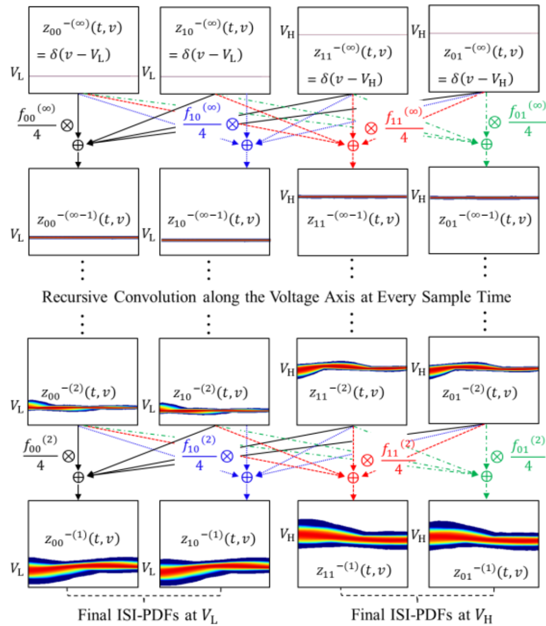


< Step 1: Analytical modeling >

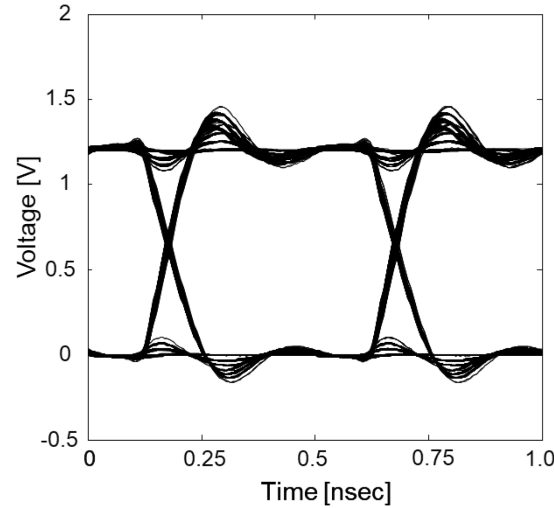
< Step 2: Statistical analysis >

- Extremely complex chip-interposer-package structure requiring heavy computational resources for the SI/PI simulation.
- Proposed a fast and accurate eye-diagram estimation method for the HBM interposer channel.

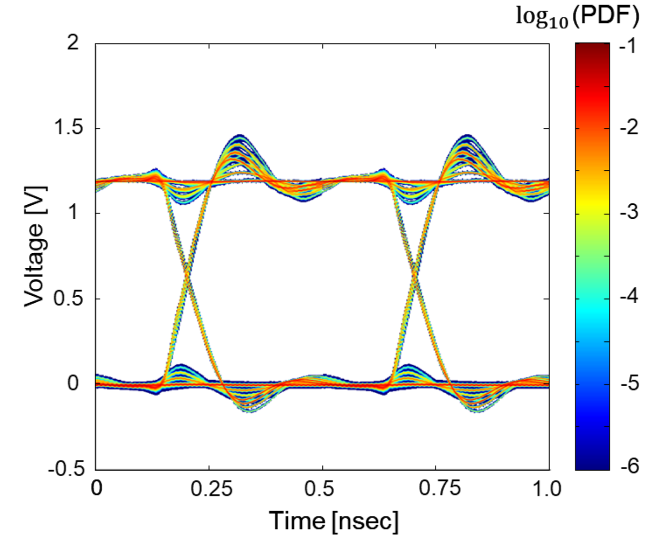
Statistical SI/PI Evaluator Development for HBM Interposer Channel (1)



<Recursive Convolution>



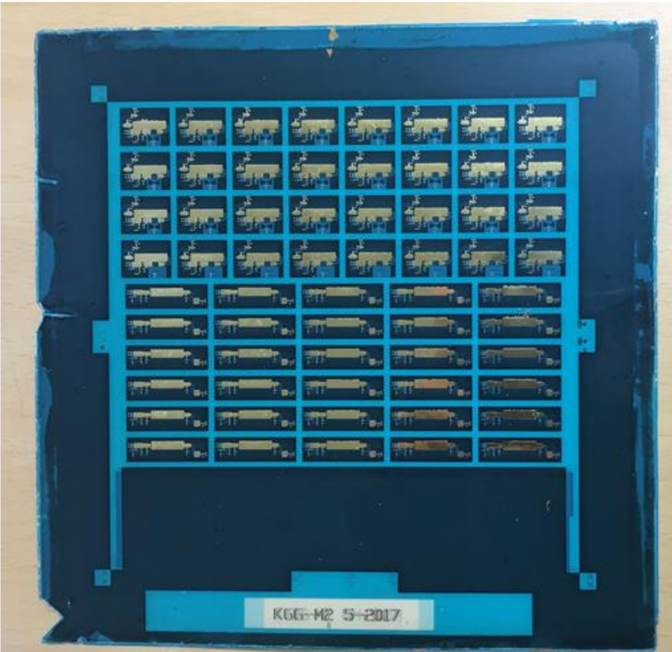
<Conventional EM + SPICE Sim.>

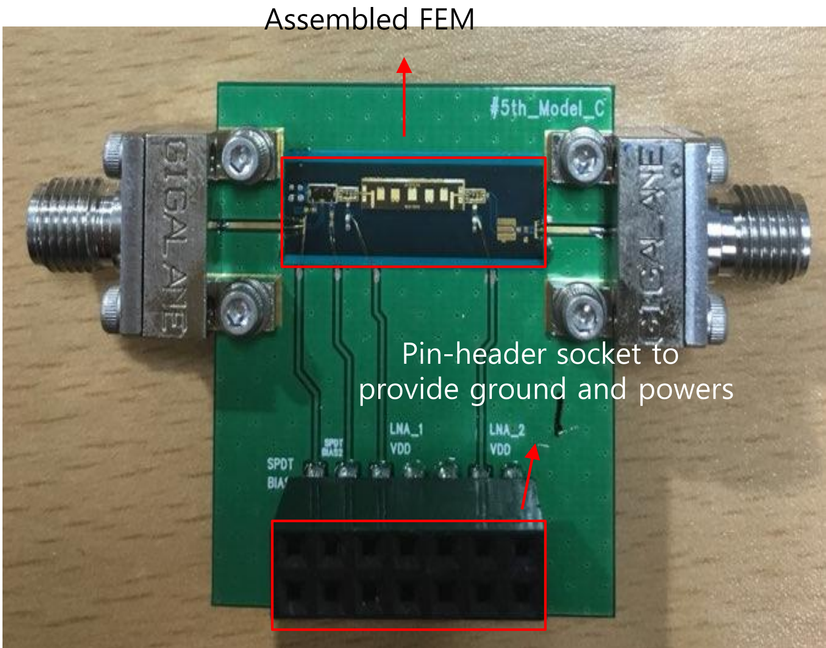


<Proposed Method>

- The proposed method is accurate but fast compared to conventional EM + SPICE simulation. The proposed method is capable of covering extremely low BER level.
- Using the proposed method, we designed interposer supporting HBM-GPU.

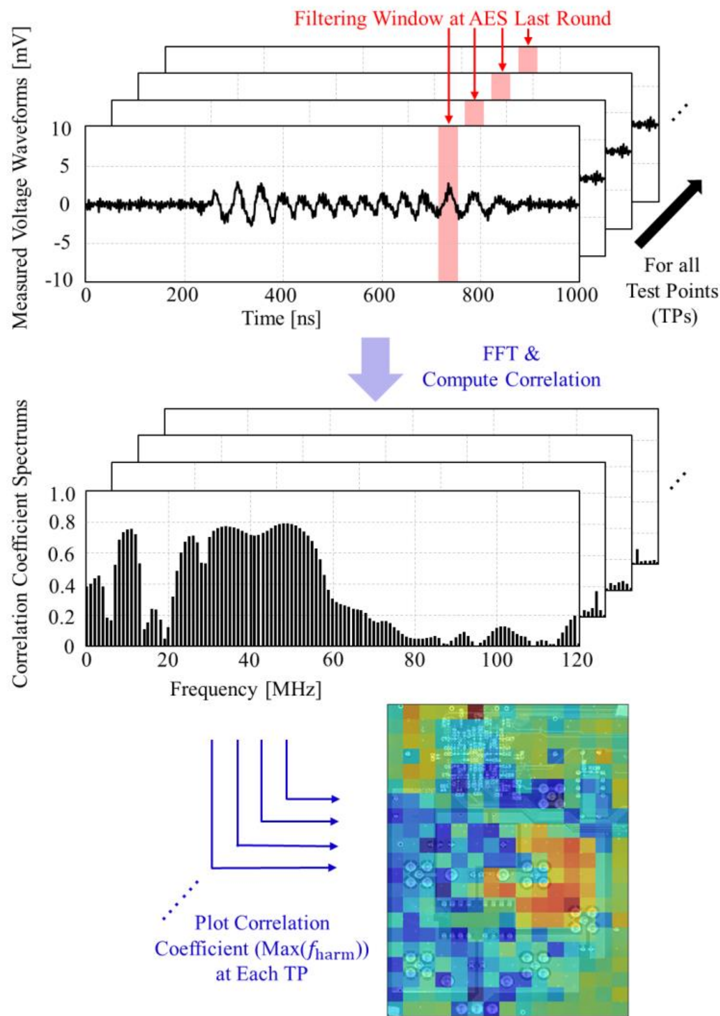
New Package Materials, Glass Package based RF FEM

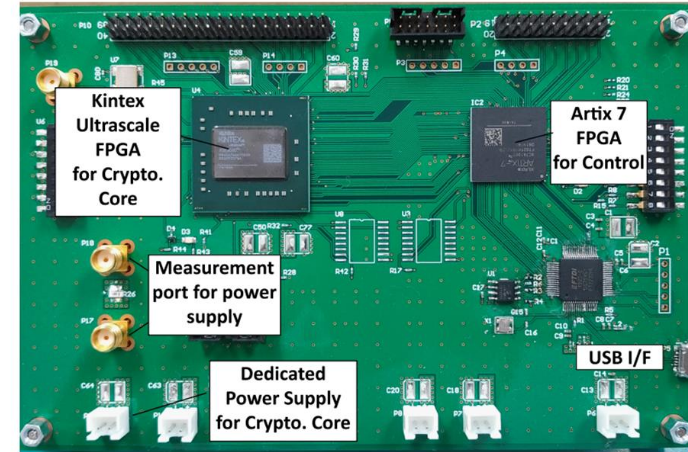


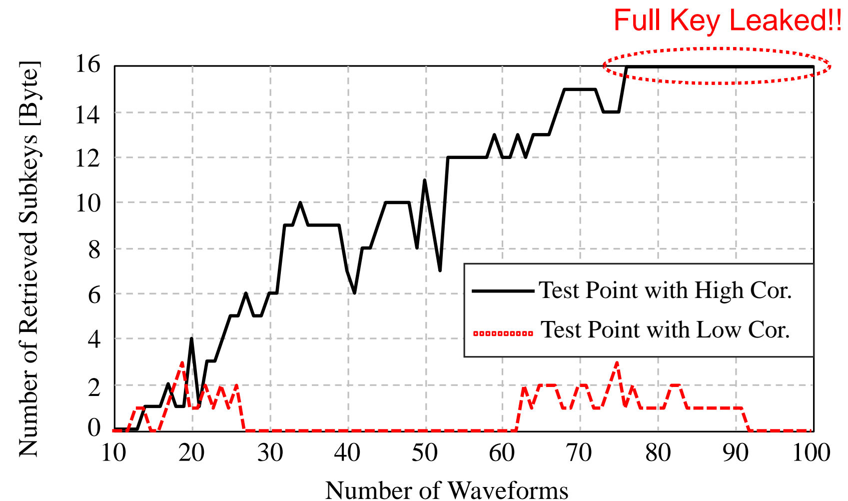


	Frequency	Gain	Noise Figure
Spec	28.0 GHz	≥ 28 dB	≤ 6 dB
Measurement results	28.0 GHz	**34.171 dB** <Spec-in>	**3.7102 dB** <Spec-in>

Interconnection Level Hardware Security







<Novel Evaluation Method>

<Developed Evaluation Platform and Analysis>

Collaboration with US Institutes

- GaTech Packaging Research Center (PRC)
  - Funded by the Korean Government for 6 Years
  - Glass package/interposer development
- Technical Consultant, Lattice Semiconductor
  - HDMI Design Lab
  - Connector-Cable-PCB-Chip Design
- Technical Consultant, Invecas Inc (USA & India)
  - Standards for HDMI 2.1
  - AI-cores, SerDes, LPDDR
- Associate Editor, IEEE Transactions on Components, Packaging and Manufacturing Technology
- Hope to collaborate again!